APPENDIX V

~~The present invention includes a memory subsystem comprising at least two semiconductor devices, including at least one memory device, connected to a bus, where the bus includes a plurality of bus lines for carrying substantially all address, data and control information needed by said memory devices, where the control information includes device select information and the bus has substantially fewer bus lines than the number of bits in a single address, and the bus carries device select information without the need for separate device select lines connected directly to individual devices.~~

~~The present invention also includes a protocol for master and slave devices to communicate on the bus and for registers in each device to differentiate each device and allow bus requests to be directed to a single or to all devices. The present invention includes modifications to prior art devices to allow them to implement the new features of this invention. In a preferred implementation, 8 bus data lines and an AddressValid bus line carry address, data and control information for memory addresses up to 40 bids wide.~~

A memory device and method for operating same is disclosed. In one particular exemplary embodiment, the memory device may comprise an array of dynamic random access memory cells, a clock

receiver to receive an external clock signal, a register to store a value, and a plurality of input receivers that includes input receivers to sample operation codes synchronously with respect to the external clock signal. A first operation code of the operation codes instructs the memory device to store the value in the register, and a second operation code of the operation codes instructs the memory device to perform a write operation. In response to the second operation code, the memory device samples write data corresponding to the write operation at a time determined using the value stored in the register. The write data is stored in the array after being sampled.